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DESIGN OF CARRY LOOK AHEAD ADDER USING SUB THRESHOLD DUAL MODE LOGIC

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Abstract- ***Sub-threshold is a new paradigm in the digital VLSI design today. In Sub-threshold region, transistors are operated in sub-threshold voltage. This paper examine the Carry Look Ahead (CLA) Adder with dual mode logic (DML)principle, in which gates are operated in sub-threshold regime and comparison of results with Conventional basic Carry look ahead adder . The number of gates in CLA is 5 including 2 XOR gates are used to perform sum & 2 NAND, an NOR gates are used to perform carry operations. It allows operation in two modes (Dual mode), very fast in the dynamic mode while energy efficient in the static mode. Critical paths are allowed to operate in dynamic mode. Non-critical paths are allowed to operate in static mode. In this result, speed, energy dissipation. Power consumption of DML based CLA is compared with conventional CLA.***

Keywords— Dual Mode Logic, Critical Paths, Dynamic Mode, Non-Critical Paths, Conventional Basic Carry Look Ahead Adder, Static Mode.

I. INTRODUCTION

Due to advancement in technology and the extension of mobile applications, power consumption is one of the considerations in VLSI digital design. Recently digital sub-threshold circuit design is a very compromising method for ultralow power applications. Circuits, operating in the sub threshold region, use a supply voltage (V_{DD}) that is less than the threshold voltages of the transistors, which provides momentous reduction of both dynamic and static power.[1].Numerous efforts in balancing the trade-off between power, area and performance have been done in the medium performance, medium power region of the design spectrum. But, not much study has been done at the two extreme ends of the design spectrum, the ultra low power with acceptable performance at one end, and high performance with power within limit at the other. One solution to achieve the ultra low power requirement is to operate the digital logic gates in sub-threshold region. Sub-threshold digital circuits are suitable only for specific application which does not need high performance, but require extremely low power consumptions. This type of applications includes medical equipments such as hearing aids and pace maker. [5]. The DML(Dual ModeLogic) Logic gates family was recently proposed in order to provide a very high level of energy-delay (E-D) optimization flexibility. DML operation allows an on the fly revolutionize between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low energy, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. A DML basic gate is based on a static logic family gate, e.g., a conventional CMOS gate, and an additional transistor whereas DML gates have very simple and perceptive structure; they necessitate an unconventional sizing scheme to achieve the desired behavior [2].In existing logic family, Simulations were performed on basic NAND/NOR gates, indicate that while operating in the dynamic mode, sub threshold DML achieves an improvement in speed of up to 10× compared to a standard CMOS, while dissipating 1.5× more power. In the static mode, a 5× reduction of power dissipation is achieved, compared to a basic domino, at the expense of a magnitude decrement in performance. [1].In this paper, we develop a basic carry look ahead adder using DML gates. So that parameters such as speed, energy dissipation of DML based Carry Look Ahead Adder are compared with conventional carry look ahead adder of 5 gates. A carry look-ahead adder improves speed by reducing the extensively used in any electronic computational devices**.**

CLA speed is frequently determined by the slowest critical carry path delay. In general, the CLA critical path is data dependent and changes during the CLA operation. However, the existing solutions improve the slowest critical path to ensure a proper operation in the worst case. Usually, these solutions improve the slowest CLA critical path delay by sizing optimization of CMOS gates or implementation with alternative design styles, such as Dynamic Logic This speed improvement is associated with a significant increase in the power dissipation of the adder. [4]. in this paper we present a novel approach for

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high performance and power efficient CLA implementation. Consistent with the proposed approach, the critical carry paths of the CLA are dynamically identified. The DML family can be switched between static and dynamic modes of operation according to system requirements. In the static (CMOS-like) mode, the DML gates feature very low power dissipation with moderate performance, while in the dynamic (NP or Domino-like) mode they achieve high performance, although with higher power dissipation. Section II introduces the reader to DML overview; operation of basic gates in sub-threshold region is described in section III. The proposed approach, including the DML based CLA architecture is described in Section IV, Section V presents simulation results and performance analysis of the proposed CLA. Section VI and concludes the paper.

II. DML OVERVIEW

Due to explore fields of varying workload, there is vast demand for high processing capabilities, as well as mobility requirements and power limitations. The DML logic was used to allow dynamic switching between static and dynamic modes of operation .The structure of the basic DML gate, shown in Fig 1, is very simple: it consists of a conventional CMOS gate with an addition Pre Discharge transistor to allow dynamic operation. During static operation, this transistor is disabled and the DML gate operates in a similar manner to a standard CMOS gate. As in other dynamic families, DML gates can be designed with or without footer. Fig 1 shows all possible DML configurations; type A with pre-charge operation and type B with discharge operation. [4].

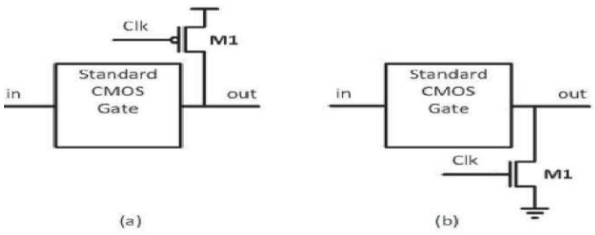

Fig 1 : DML gate a)Type A topology b)Type B topology

To operate the gate in the dynamic mode, the Clk is assigned an asymmetric clock, allowing two distinct phases: precharge and evaluation. In precharge phase, the output is charged to high/low, depending on the topology of the DML gate. In the consequent evaluation phase, the output is evaluated according to the values at the gate inputs. The DML topologies, marked *Type A* and *Type B*, are illustrated in Fig. 1. Type A has an added p-MOS transistor that precharges the output to a logical "1" during the precharge phase. Type B has an added n-MOS that precharges the output to a logical "0." Dynamic logic gates are often implemented using a footer, which requires an additional transistor. The footer is used to decrease precharge time by eliminate the ripple effect of the data advancing through the cascaded nodes and allowing faster precharge. Switching the DML gate to operate in CMOS-like operation is discerning: the global Clk should be fixed high for Type A topology and it should be low for Type B topology. Hence the gate has a similar topology to CMOS, with the exception of for the extra parasitic capacitance, which is usually negligible. Creating a DML node based on a CMOS gate is also very simple: in Type A gates, adding an additional n-MOS transistor as footer and in Type B gates a p-MOS transistor as a header is added. [1].

2.1 Static logic or standard CMOS logic operation

Static logic circuits provides adaptable implementation of logic functions based on static, or steady-state, behavior of simple CMOS structures. A distinctive static logic gate generates its output levels on condition that the power supply is provided. This approach, however, may have need of a large number of transistors to implement a Static CMOS logic are function, and cause considerable time delay.

Basic features of

- Very low static power dissipation.
- High noise margins (full rail to rail swing).
- Low output impedance, high input impedance
- No steady state path between V_{DD} and GND.
- Delay is function of load capacitance and transistor resistance.
- Comparable rise and fall times (under the appropriate transistor sizing conditions) [6].

2.2 Dynamic Logic operation

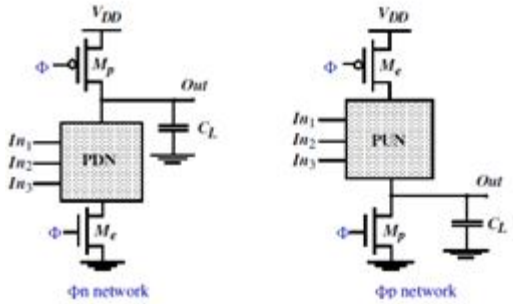

Fig 2 : Dynamic CMOS

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Precharge- In the dynamic CMOS, PMOS transistor is precharge gate and NMOS transistor is evaluation gate .when clock is zero(CLK=0) output node is precharge to V_{dd} by the PMOS transistor Mp while evaluate NMOS transistor is off so the pull down path is disabled. Evaluation transistor (NMOS) eliminates any static power dissipation that would be consumed by the prechargeperiod.

Evaluation– when CLK=1 precharge transistor (Mp) is off and evaluation transistor is on during this time output is discharge based on input value. If the input is such that PDN conduct then a low resistance path exists between output and GND and output is discharged to GND. If the PDN is off then precharge value is stored on the output capacitance CL. Once output node is discharge then it cannot be charged again till the next precharge operation. Output can be high impedance state during the evaluation period if the pull down network is off [7].

Advantages over static logic

- Avoids duplicating logic twice as both N-tree and P-tree, as in standard CMOS.
- Typically can be used in very high performance applications
- Very simple sequential memory circuits; agreeable to synchronous logic
- High density achievable
- Consumes less power (in some cases)

Disadvantages compared to static logic

- Problems with clock synchronization and timing
- Design is more difficult.
- Dissipates less Energy in the static mode

2.3 DML (Dual Mode logic)

A DML gate can be sized to optimize speed, area or power. In this paper, the DML gates were optimized to improve speed in the dynamic mode, while maintaining a minor degradation performance during static operation [4]. Since the performance in the dynamic mode is mainly determined by the evaluation speed, the evaluation is always performed through a network of parallel transistors, and minimal sized transistors are utilized in the active self-restore network.

This allows capacitance reduction at the gate output, especially for the gates with a large fan-in. The strength of the evaluation network is set to be equivalent to one minimally sized NMOS transistor, similarly to standard CMOS methodology. DML topology can be constructed with or without footer and the preferred topology depends on the supply voltage, power limitations and required performance. The footed configuration proposes the following features: zero short circuit power during precharge, short pre-charge phase and robustness to process variations. precharge, due to the ripple evaluation chain effect. Other disadvantages of un-footed topology are a longer pre-charge period, higher PV sensibility and lower robustness. However, the main advantage of the un-footed topology is the small capacitance (gate and drain), resulting in faster evaluation time and therefore improved gate speed.

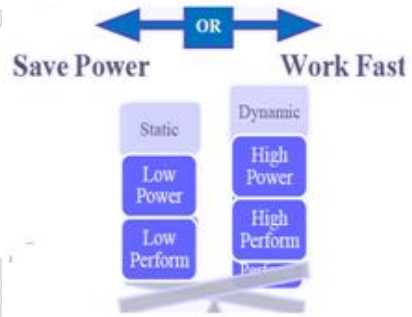

Fig 3: Dual Mode Logic

III. BASIC GATES IN SUB-THRESHOLD DML

The basic concept behind the DML is to combine the traditional CMOS logic (or any other static logic) with a dynamic logic. An additional footer /header transistor (connected in series to an evaluation path) is optional to ensure a correct interface with other gates. The design methodology that should be used when designing a DML gate is to place the precharge transistor in parallel to the stacked transistors. Thus, the evaluation is performed with the parallel transistors and, therefore, it is faster.

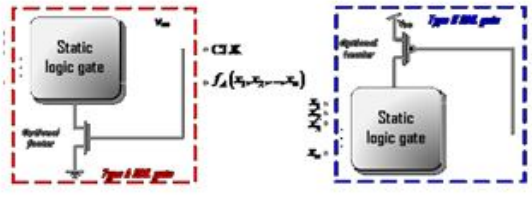

Fig 4 : DML gate operation

The stacked transistors will be sized to minimal widths to reduce intrinsic capacitances, increasing dynamic operation performance over reduced static operation performance. This

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sizing strategy also results in reduced energy dissipation, as compared to conventional static CMOS gates. The precharge transistor is also minimum sized to decrease leakage currents during static operation and evaluation. Note, all gates can be designed either as Type A or Type B. The optimal design methodology when designing with DML gates is to cascade connects Type A and Type B gates, exactly like in np-CMOS gates. Even though this design methodology will allow maximum performance, minimize area, and maximize power efficiency, it is possible to connect gates of the same type by using an inverter buffering between them, in a similar way it is done in domino logic. Connecting gates of the same type without inverters is also possible when a footer/header is used at each stage, however, this structure will cause glitching after precharge ends and until the evaluation data ripples through the chain. These are standard problems when designing with dynamic gates [1]. However in contrast to the standard dynamic logic, DML's inherent keeper helps recover the logical value.

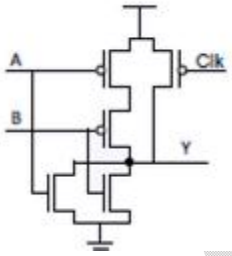

Fig 5 : NOR gate using DML

A gate is either precharged to V_{DD} or dis/precharged to 0 V, and after a predefined period, the output voltages of the different gates are compared. Dynamic gates suffer from charge leakage, which becomes more severe in sub-threshold due to long static periods. This analysis takes into account all the parasitic leakages and approximates the robustness of the dynamic gate to hold a logical 0 or a logical 1.All the test gates were examined and characterized in a standard low-power 80-nm process. Power supplies between 150 mV and 600 mV were tested for energy estimation. We use 300mv V_{DD} for supply voltage whereas 285 mV for CMOS, 470 mV for dynamic logic gates. The operation frequency of the entire chain is $f = 1/T$, frequency is calculated by, $(T_{LH}+T_{HL}) \div 2$. After the precharge phase, the output of a dynamic NOR gate is high, and when no switching occurs, it literally gives $t$plh = 0. When switching does occur, the output capacitance $C_L$is discharged through the pull-down network. Supply voltage is between the ranges of 200-500 mV, strong inversion operations, measurements are performed with supply voltages varying from 0.4V to 1.1V.In DML operation in the dynamic mode achieves a much better performance, it consumes more power than CMOS. On the other hand, DML operation in the static mode is power efficient and allows a power reduction of up to 33% and 45%, compared to CMOS and dynamic DML, respectively.

IV. DESIGN OF CLA USING SUB THREHOLD DML

In proposed system, we implement Sub-threshold Dual Mode Logic methodology in CLA. The experimental result shows performance of our proposed method. The novel Dual Mode Logic (DML) family of logic gates was recently as an energy efficient alternative to standard CMOS logic. DML and its accompanying design methodology present a unique concept that enables an on-the-fly tradeoff between high performance (Dynamic mode) and energy efficient (Static mode) operation. The DML methodology allows real time switching between these modes of operation from the scope of a single gate and up to a complete design block. This added flexibility provides the means to meet the delay requirements while minimizing power dissipation. The DML family, which is fully compatible with any standard logic process, was demonstrated to be fully functional at all operational regions from STV through NTV, and up to nominal supply voltages.

In this paper, we design one basic carry look-ahead adder with the principle of Dual Mode Logic and transistors are to be operated in sub-threshold regime.i.e (threshold voltage of PMOS and NMOS is lesser than threshold voltage of conventional gates).Hence this implementation proceeds reduced power consumption. A Ripple Carry Adder (RCA) is a very area-efficient adder design. Unfortunately, it is also slow. The maximum delay of an RCA is from the carry-in input to the carry out, passing through each full adder along the way. As with many design problems in digital logic, we can make tradeoffs between area and performance (delay).

In the case of adders, we can create faster (but larger) designs than the RCA. The Carry Look-ahead Adder (CLA) is one of these designs. We separate the carry chain (the logic that propagates the carry through the full adders of the RCA) from the sum logic. Nowadays, Power consumption is one of the primary focus of VLSI attention. To achieve low power requirement, we can operate the digital logic gates in sub-threshold region. In this paper, we have to implement this application in basic Carry Look Ahead Adder to achieve high speed. Here we analyze DML in single bit Carry-Look Ahead Adder with 5 gates to increase speed. The critical path is

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identified according to the inputs during operation and operated in dynamic mode .Rest of the circuit operates in the DML static Low Energy mode.

For basic carry look ahead adder design,

following equationaare used to calculate sum,carry bits.

$P^i = A^i \oplus B^i$ Carry propagate

$G^i = A^i \cdot Bi$ Carry generate.

Both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay

$S^i = P^i \oplus C^{i-1}$

$C^{i+1} = G^i + P^i \cdot C^i$

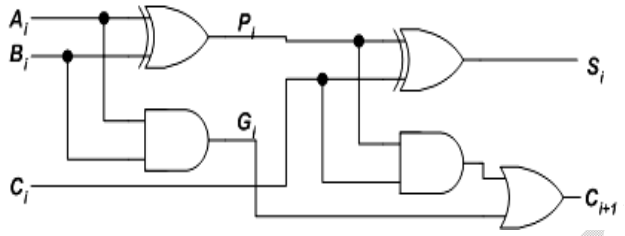

Fig 6 : Logic Diagram Of Carry Look Ahead Adder

For higher bits of operation,Dual mode logic is switched to dynamic mode due to internal carry propogation.it can be understandable by following table.

Table 1.Dynamic activation

X_i	Y_i	C_{in}	C_{next}	Dynamic activation is needed	NOR(Xi,Yi): When0 route is dynamically activated	False dynamic activation
0	0	0	0		1	
0	0	1	0		1	
1	0	0	0		0	Yes
1	0	1	1	Yes	0	
0	1	0	0		0	Yes
0	1	1	1	Yes	0	
1	1	0	1	Yes	0	
1	1	1	1	Yes	0	

The critical path of CLA is the longest carry route.The critical path is identified according to the inputs during operation and operated in dynamic mode **.**For single bit operation.

P1=A1⊕ B1

G1=A1.B1

S1=A1 ⊕ B1 ⊕C0

C1=G1 +P1· C0

C1= A1.B1 +P1· C0

Hence 2 bit 2 XOR gates,2 AND,OR gates are implemented in DUAL MODE LOGIC.

Processing steps:

1.Construct conventional NAND gate.
2.Construct DUAL mode logic NAND gate.
3.Read the power,delay values from output.
4.Similiarly DML based XOR,NOR gates are implemented.
5.Design carry look ahead adder based on dual mode logic.
6.Design conventional carry look ahead adder.
7.Analyse the results of carry lookahead adder on both types.

For higher order bits,initial carry is given to static path(non critical path).inner bit carry are propogated to dynamic path.(critical path).

PERFORMANECE PARAMETERS OF DUAL MODE LOGIC CLA:

The critical path of CLA is the longest carry route. The critical path is identified according to the inputs during operation and operated in dynamic mode (requires additional control circuitry).Generating and propagating in the context of binary addition. *SPEED*: The speed of a digital circuit is very important, as it will determine the maximum frequency at which it can work. Provides look ahead carries across a group of four ALUs Multi-level look ahead high-speed arithmetic operations over long word lengths. Speed of conventional carry look adder is compared with 3 bit dual mode logic based carry look-ahead adder.

ENERGY DISSIPATION: CMOS circuits dissipate no static (DC) power, since in the steady state there is no direct path from V_{DD} to ground. The energy dissipation is greatly reduced by shutting down the idle power gating CLA blocks. Leakage currents and substrate injection currents which leads to static power dissipation in CMOS circuits.

One of the dynamic components of power dissipation arises from the transient switching behavior of the CMOS devices. PERFORMANCE ANALYSIS: In static mode, low voltage DML gates achieve very low Energy consumption with moderate performance. In dynamic mode they achieve high performance, albeit with higher Energy consumption. Various parameters describe the performance of carry look ahead which we designed is more convenience the conventional adder.

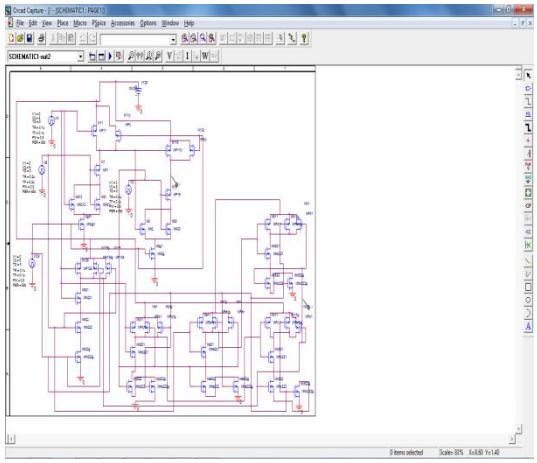

Fig 7 : Circuit diagram of proposed CLA

V. SIMULATION RESULTS

Simulations are carried out in PSPICE for both conventional, DML based CLA.Results Show that, reduced power consumption, dissipation.

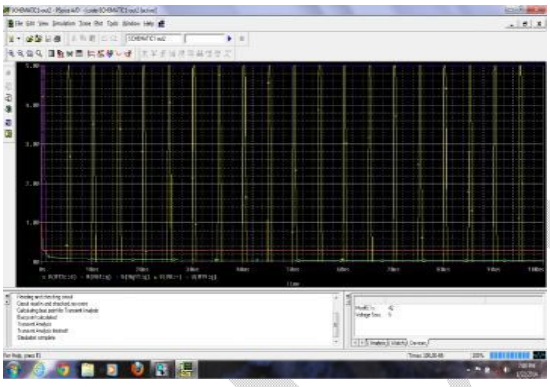

Fig 8 : Output voltage wave for mof DML based Carry look Ahead Adder

Table 2. Comparison of carry looks ahead adder

	POWER DISSIPATION (mw)	POWER CONSUMPTION	SPEED (us)
CLA	2.9*10^-8	600mv-1v	2.15
DML CLA	6.57*10^-10	500	1.25

VI. CONCLUSION

A dual-mode logic gate, for selectable operation in either of static and dynamic modes, includes: a static gate which includes at least one logic input and a logic output; a mode selector, configured for outputting a turn-off signal to select static mode operation and for outputting a dynamic clock signal to select dynamic mode operation; and a switching element associated with the mode selector static gate, comprising a first input connected to a constant voltage, a second input for inputting the mode selection signal from the mode selector, and an output connected to a logic output of the static gate. In this project, we implemented the dual mode CMOS in carry look ahead adder logic circuit. Simulation results shown that, power consumption, speed, power dissipation are compared with conventional carry look-ahead adder.

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